Customized TTA Processor for efficient implementation of variable length FFT in SDR Systems

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Introduction

- Fast Fourier Transform (FFT) is one of the most used algorithms in many applications, in particular, in Software Defined Radio (SDR) systems.
- Very tight real-time constraints under pressure of low-cost and low-power implementations should be met.
- In SDR, HW and SW should be optimized simultaneously to achieve these tight requirements.
- One of the most advanced HW/SW co-design approaches is provided by Transport-Triggered Architecture (TTA) based Co-design Environment (TCE) toolchain developed in Tampere University of Technology.
- Recently, based on this technology, a programmable implementation of FFTs of variable sizes $N=4^m2^n$ was proposed that has shown competitive performance to pure HW implementations.
- In this work, we propose a new TTA for implementation of mixed-radix 4/2/3 FFTs of variable sizes $N=4^m2^n3^l$ to support all sizes needed in LTE.
- Compared to the previous design, the proposed architecture achieves not only higher flexibility, but also improves the performance

The underlying FFT algorithm

To compute Discrete Fourier Transform (DFT)

$$\mathbf{y} = F_N \mathbf{x}\ , \quad F_N = \left\{ W_N^{pq} \right\}_{p,q=0}^{N-1}\ , \ W_N = \exp\left(-\frac{2p\sqrt{-1}}{N} \right)$$

of the size $N=4^m 2^n 3^l$ we use the following formula:

$$F_{4^m 2^n 3^l} = \left[\left(F_3 \otimes I_{lN} \right) T_{lN}^{N} \right] I_3 \otimes \left\{ \left(F_2 \otimes I_M \right) T_M^M \left[\prod_{i=1}^{m} (I_{2^k} \otimes I_{4^{i-1}} \otimes F_4 \otimes I_{4^{m-i}})(I_{2^k} \otimes I_{4^{i-1}} \otimes T_{4^{m-i}}^{4^{m-i+1}}) \right] \right\} R_{4^m 2^n 3^l}$$

where $M = N/3$,

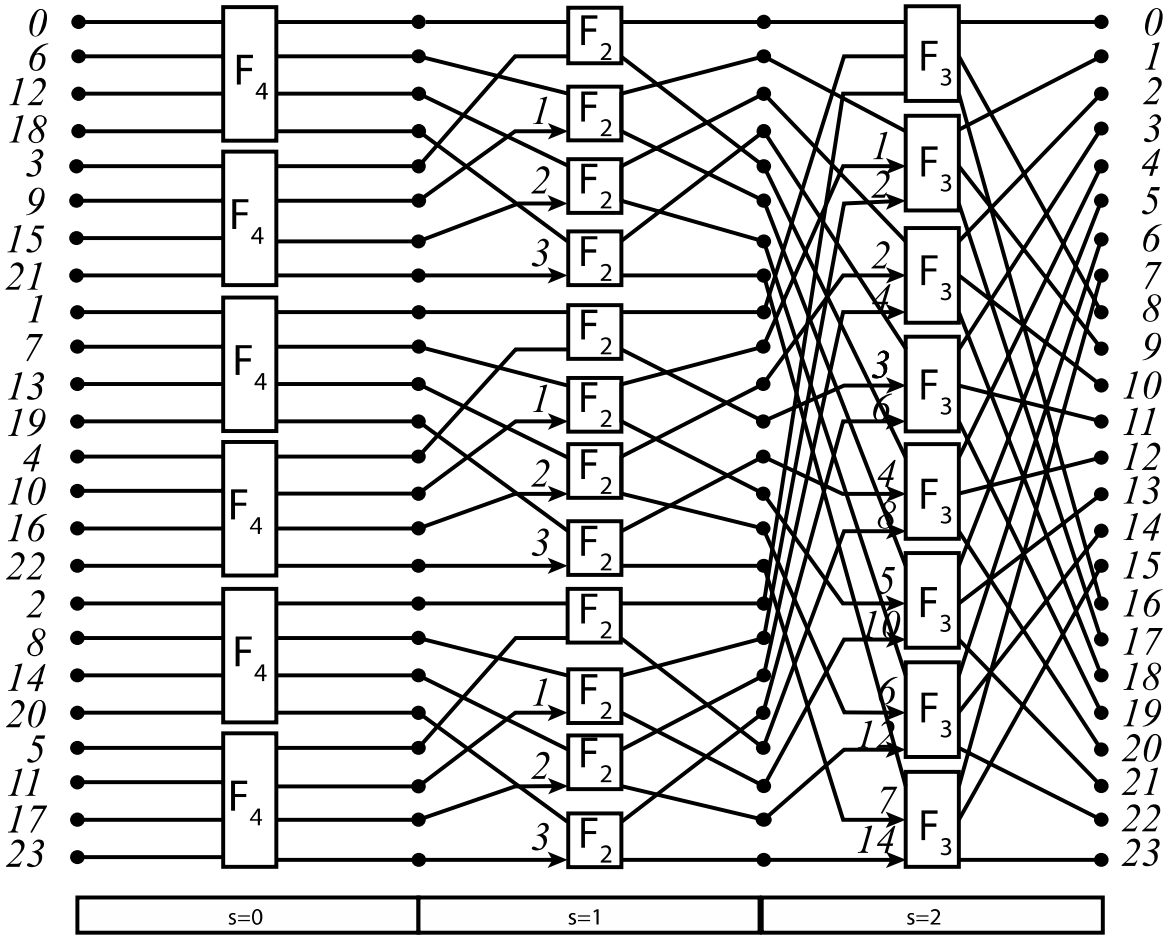
$$R_{4^m 2^n 3^l} = \left(I_{3^l} \otimes \left(I_{2^n} \otimes \left(\prod_{i=1}^{m} I_{4^{m-1}} \otimes P_4^{4^m} \right) \right) \right) P_{3^l}^{N}$$

P_N^k is stride by *k* permutation matrix of order *N*,

$$T_s^{rs} = \oplus_{i=0}^{r-1} (D_s^{rs})^i, where\ D_s^{rs} = diag(W_s^0, W_s^1, \ldots, W_s^{s-1})$$

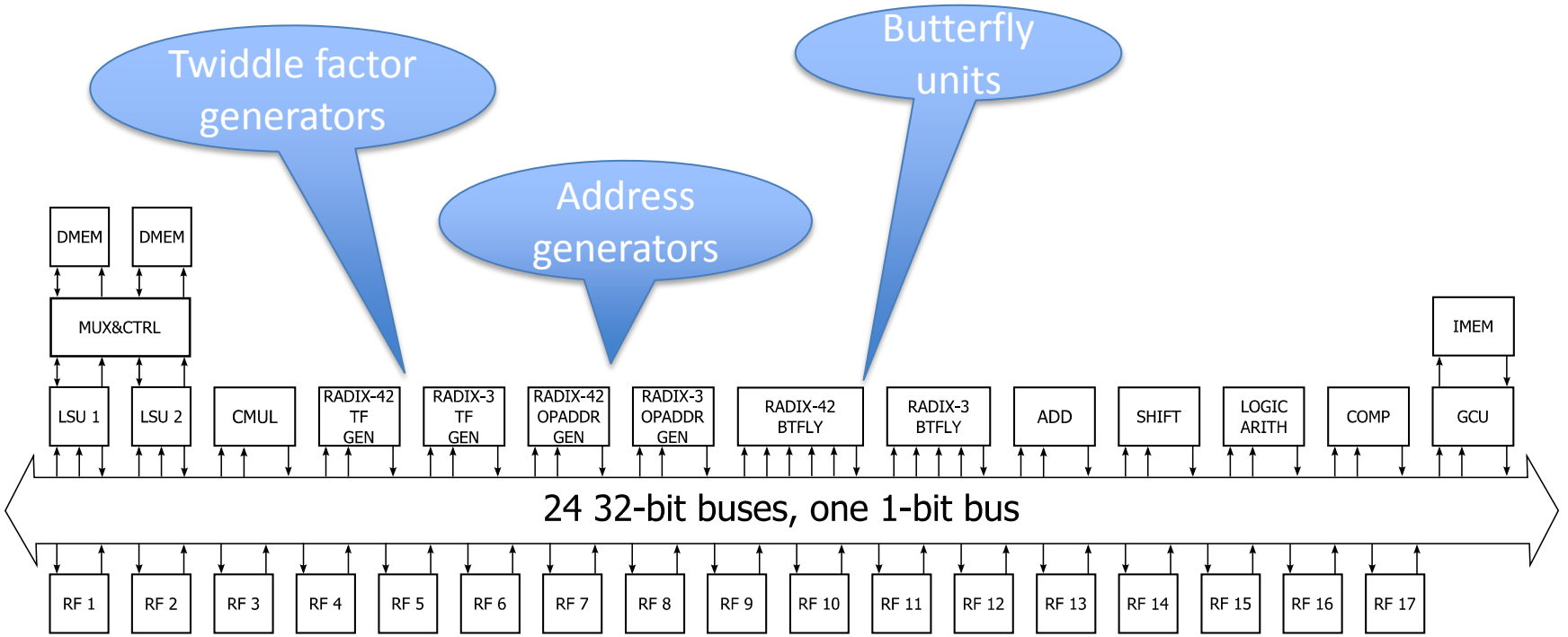
The underlying FFT algorithm

$$N = 24 = 4 \times 2 \times 3$$



- ✓ Three FFTs of order N=8 followed by eight FFTs of order three
- ✓ Radix-4/2 designs can be utilized:
  - ✓ However, we modify those to further improve performance
- ✓ Complemented with the design of radix-3 FFT

Transport-Triggered Architecture (TTA) for radix-4/2/3 FFT



In TTA, operations are implemented by passing through chain of Functional units connected by buses

Twiddle factor generation

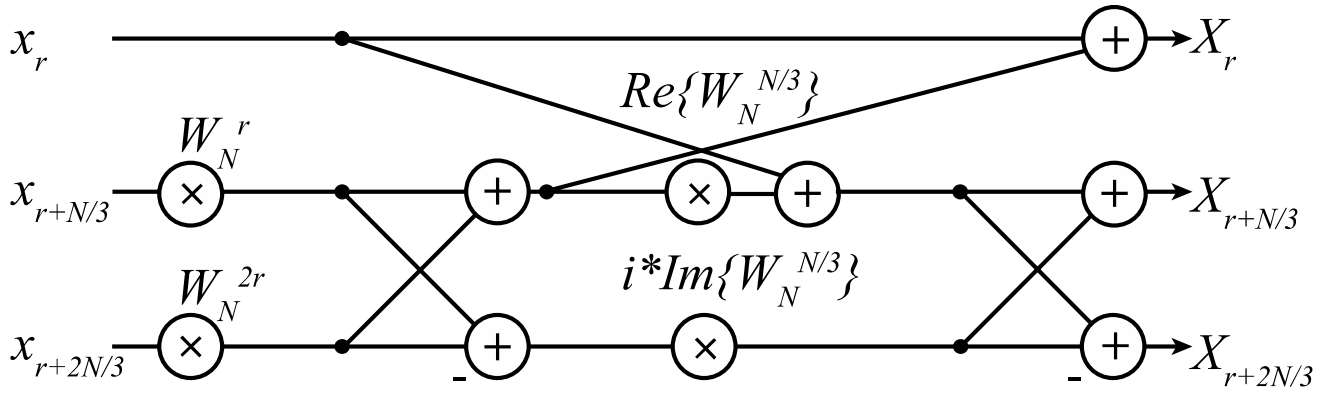
- Total of N Twiddle Factors (TF) $W_N^p,\ p = 0,\ldots,N-1$ are used in FFT.
- In our implementation only N/8 of TFs are stored in a ROM.
- When a TF is needed it is obtained from one of the stored ones by simple manipulations:
  - exchange,
  - addition,
  - subtraction
- The simplified logic of the unit shortens the critical path of the whole processor allowing to clock it faster if needed

Operand access

- Address generators obtain operand accesses by simple rotations of linear address indices.
- In our approach we use FFT structure where:
  - the first $n+m$ stages implement 3^l $(l=0,1)$ separate FFTs of order $4^m 2^n$;
  - If $l=1$, the last stage implements $4^m 2^n$ separate FFTs of order 3.
- Thus addressing in the first FFT stages are the same as in radix-*4/2* FFTs:
  - existing addressing solutions can be reused
- Addressing of the last stage is easy since addresses of operands differ by *N/3*, which is a power of two:
  - can be implemented by simple logical OR operation.

Butterfly units

- Radix-4/2 butterflies are the same as in precious design:
  - efficient reuse;
- Radix-3 butterfly is newly designed:



Synthesis results

	mixed-radix-4/2	mixed-radix-4/2/3
supported FFT sizes	$64 - 16384$	$128 - 2048/1536$
cycle count	$207 - 114722$	$544 - 12335$
execution time	$828ns - 459\mu s$	$1.3 - 30.8\mu s$
	$@250MHz$	$@400MHz$
max. clock freq.	$250MHz$	$400MHz$
Area [kgates]		
Core	38	46
Imem	2	3
Dmem	240	60
Total	280	109
1024-point FFT		
cycle count	5160	5180
1536-point FFT		
cycle count	N/A	9324
2048-point FFT		
cycle count	12332	12345

- ✓ Increased flexibility (radix-3 support)
- ✓ Reduced area (280 → 109)
- ✓ Faster max clock (250 → 400)
- ✓ Similar cycle counts

130nm standard cell technology

Conclusions

- Programmable radix-4/2/3 FFT implementation was proposed that supports variable lengths FFT of sizes needed in LTE
- The processor improves the performance of the previous radix-4/2 design, that has shown competitive performance to pure HW solutions