# Cooperative Actor-Oriented Synthesis for FPGA-Based MIMO Detection

Yun Wu, John McAllister, Peng Wang
Queen's University Belfast

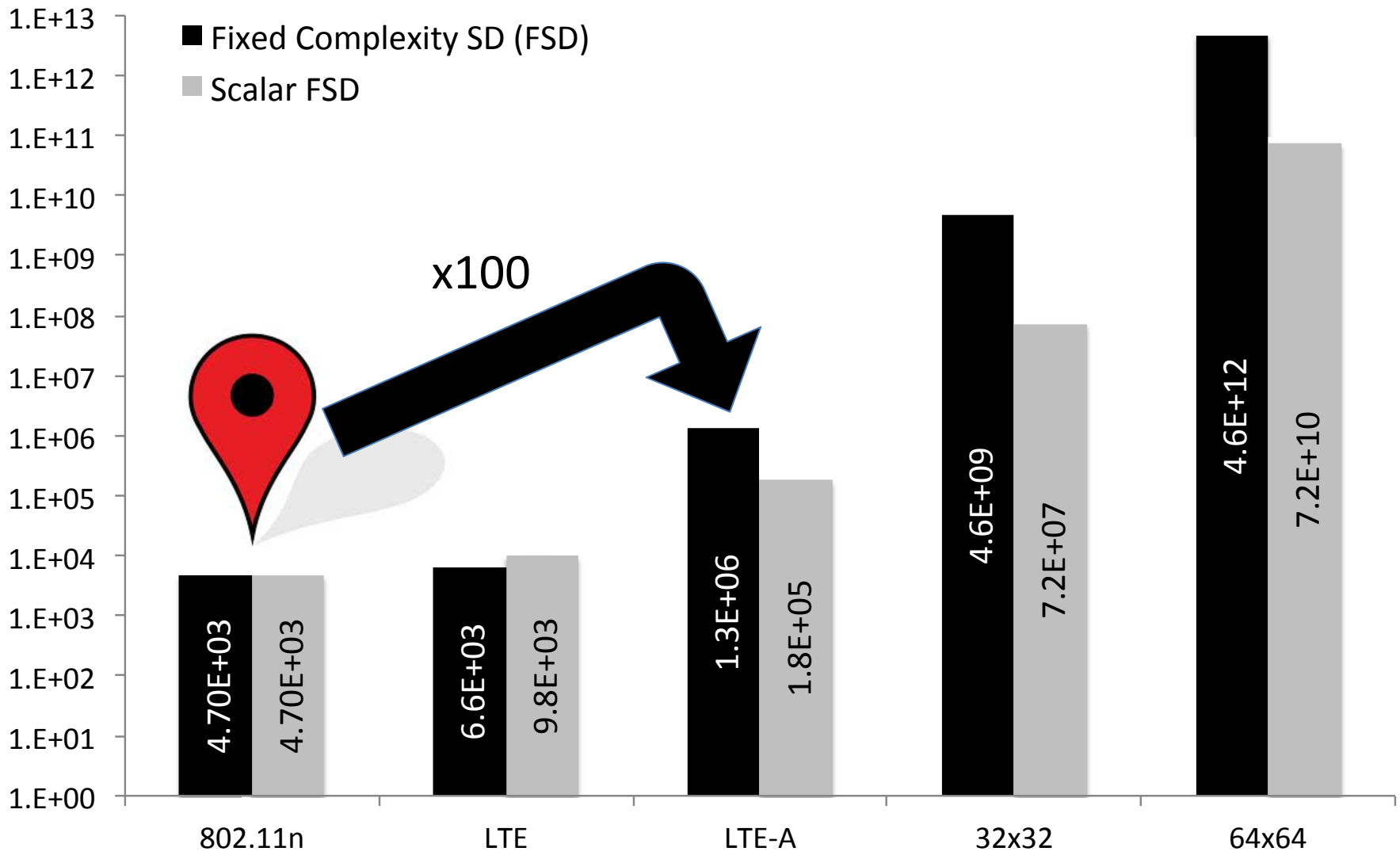
"...making your phone at least 100 times faster than today's 3G smart phones...IMT-Advanced will use radio-frequency spectrum much more efficiently, making higher data transfers possible on lesser bandwidth. This will enable mobile networks to face the dramatic increase in data traffic that is expected in the coming years"

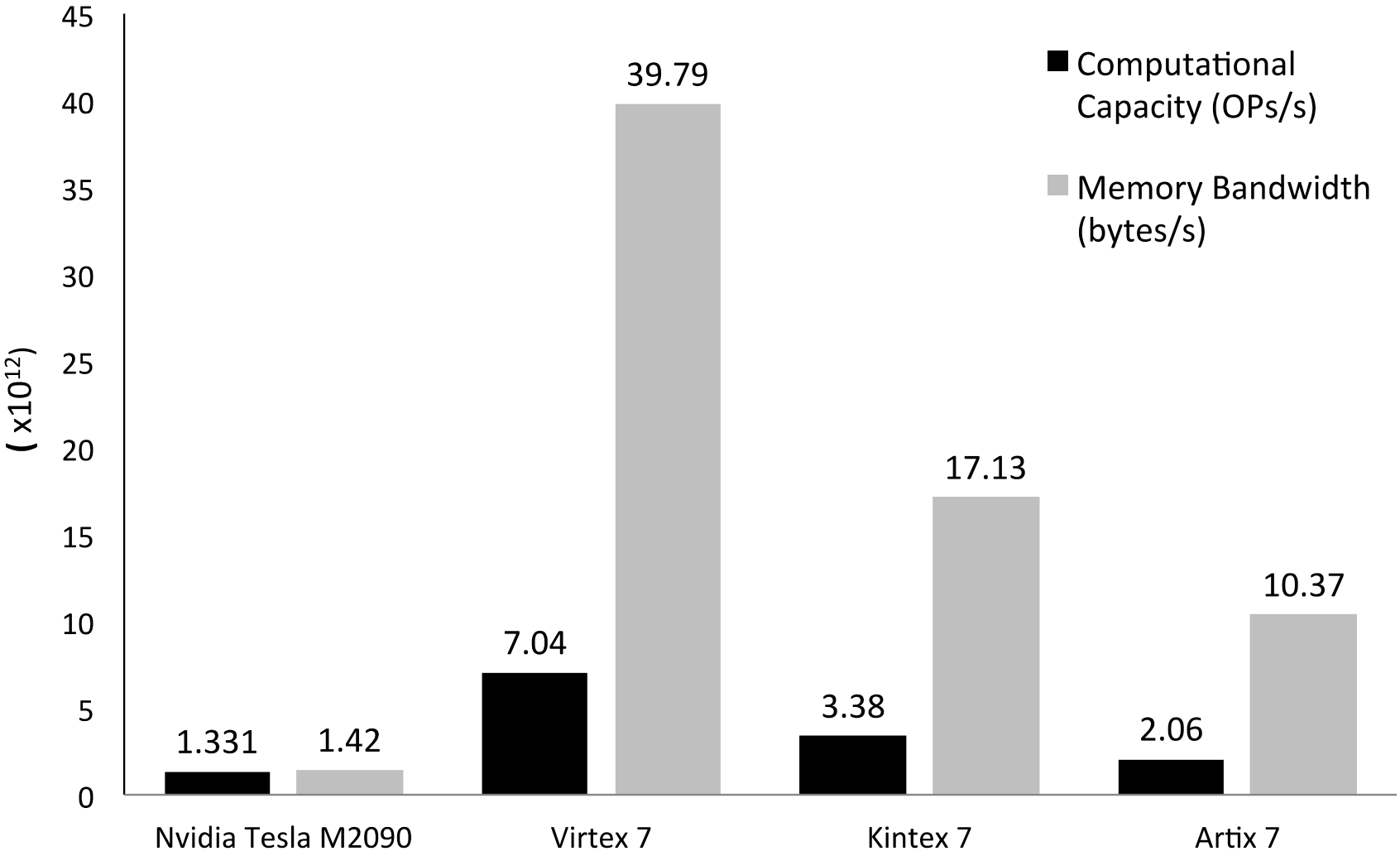
International Telecommunications Union: “IMT-Advanced Standards Announced for Next-Generation Mobile Technology”. 2012.

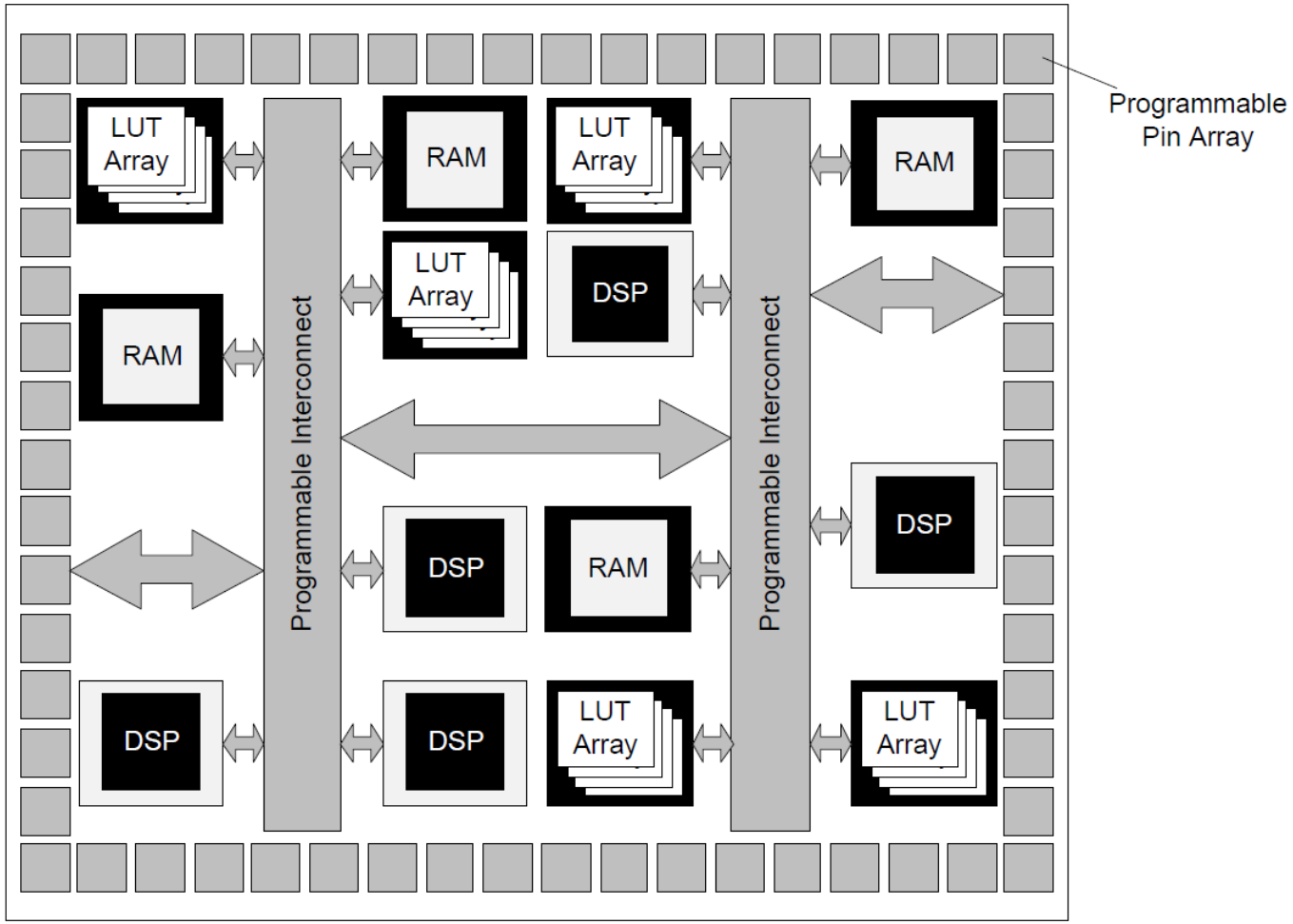
“The challenge in LTE-Advanced system design is therefore to devise a MIMO detector that achieves performance close to ML, while still incurring computational cost within the reach of current hardware”

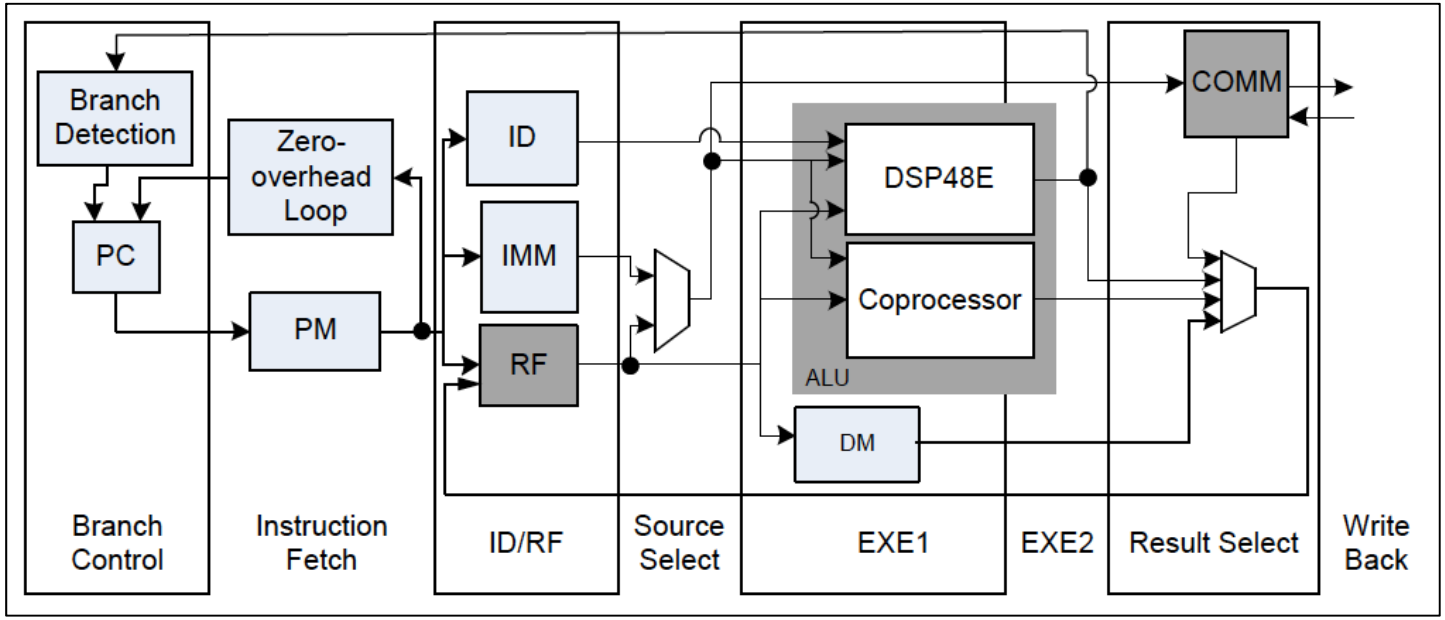
D. Bai, IEEE Communications Magazine, February 2012.

$$O(M_t^4) + O(2^{M_c + \lceil M_t - 1 \rceil})$$

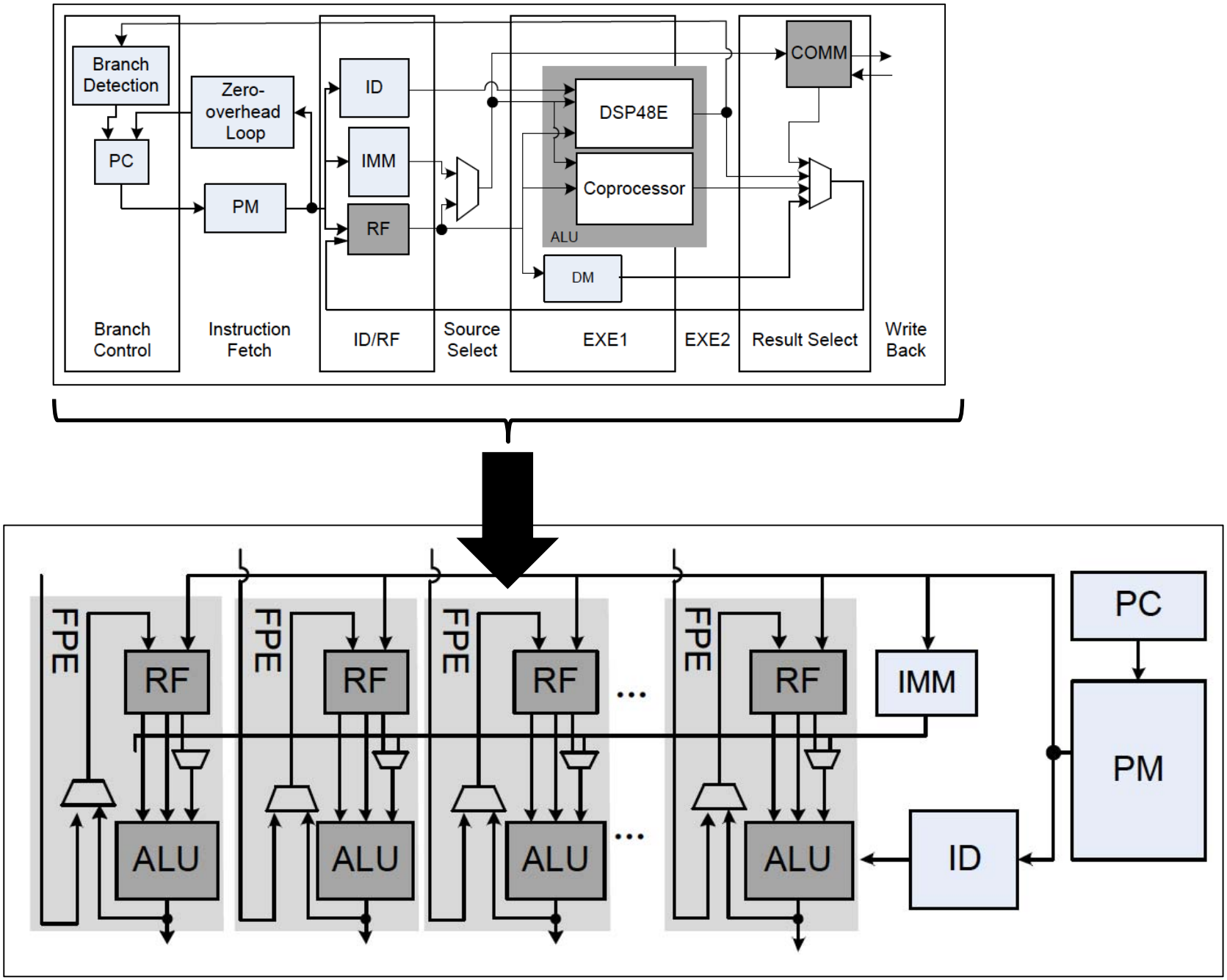

Fixed Complexity SD (FSD)
Scalar FSD
x100
1.E+13
1.E+12
1.E+11
1.E+10
1.E+09
1.E+08
1.E+07
1.E+06
1.E+05
1.E+04
1.E+03
1.E+02
1.E+01
1.E+00
4.70E+03
4.70E+03
6.6E+03
9.8E+03
1.3E+06
1.8E+05
4.6E+09
7.2E+07
4.6E+12
7.2E+10
802.11n
LTE
LTE-A
32x32
64x64

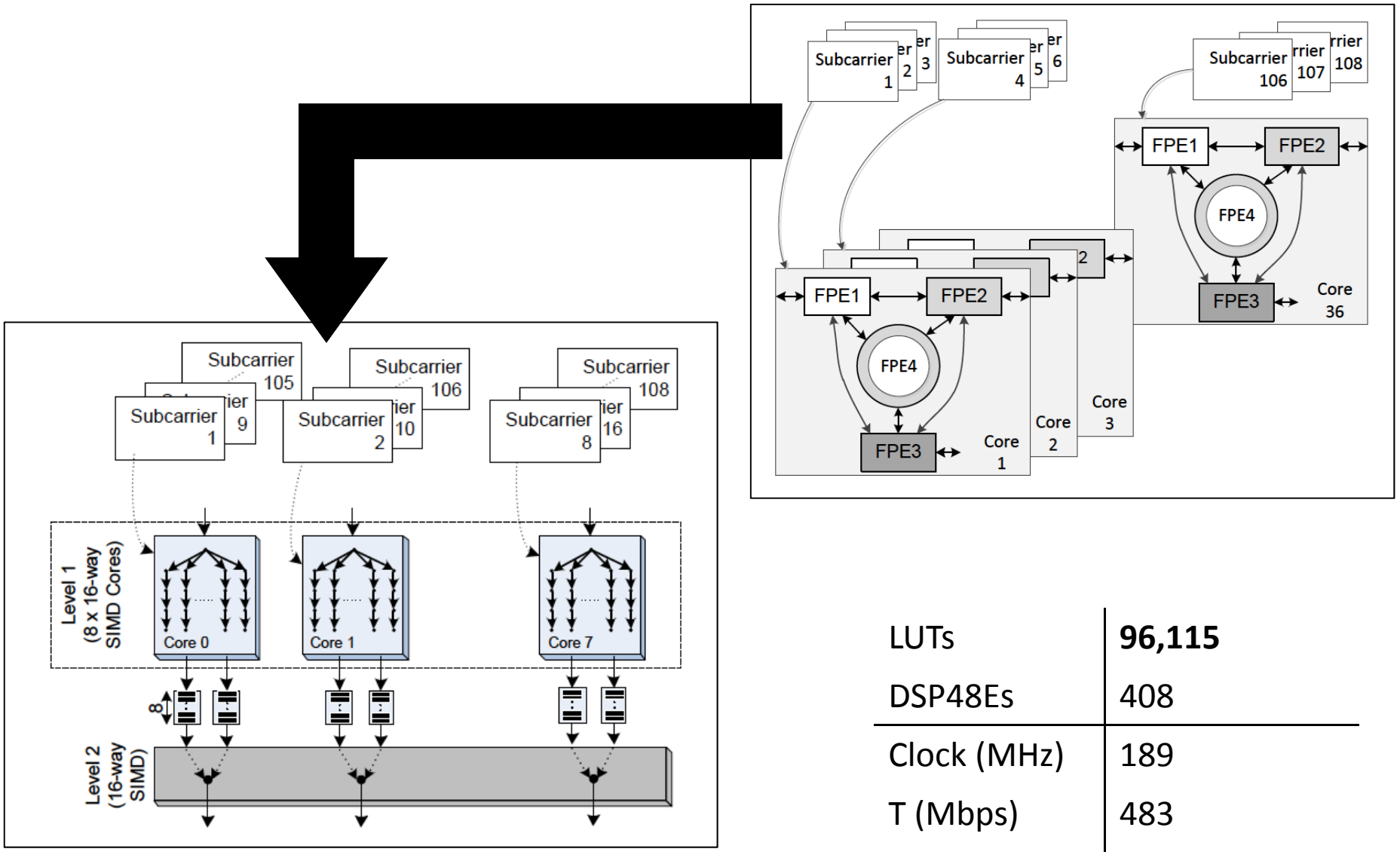

45
40
35
30
25
20
15
10
5
0
( x10^12)
39.79
17.13
10.37
7.04
3.38
2.06
1.331
1.42
Computational Capacity (OPs/s)
Memory Bandwidth (bytes/s)
Nvidia Tesla M2090
Virtex 7
Kintex 7
Artix 7


LUT Array
RAM
LUT Array
RAM
LUT Array
DSP
RAM
Programmable Interconnect
Programmable Interconnect
DSP
DSP
RAM
DSP
DSP
DSP
LUT Array
LUT Array
Programmable Pin Array

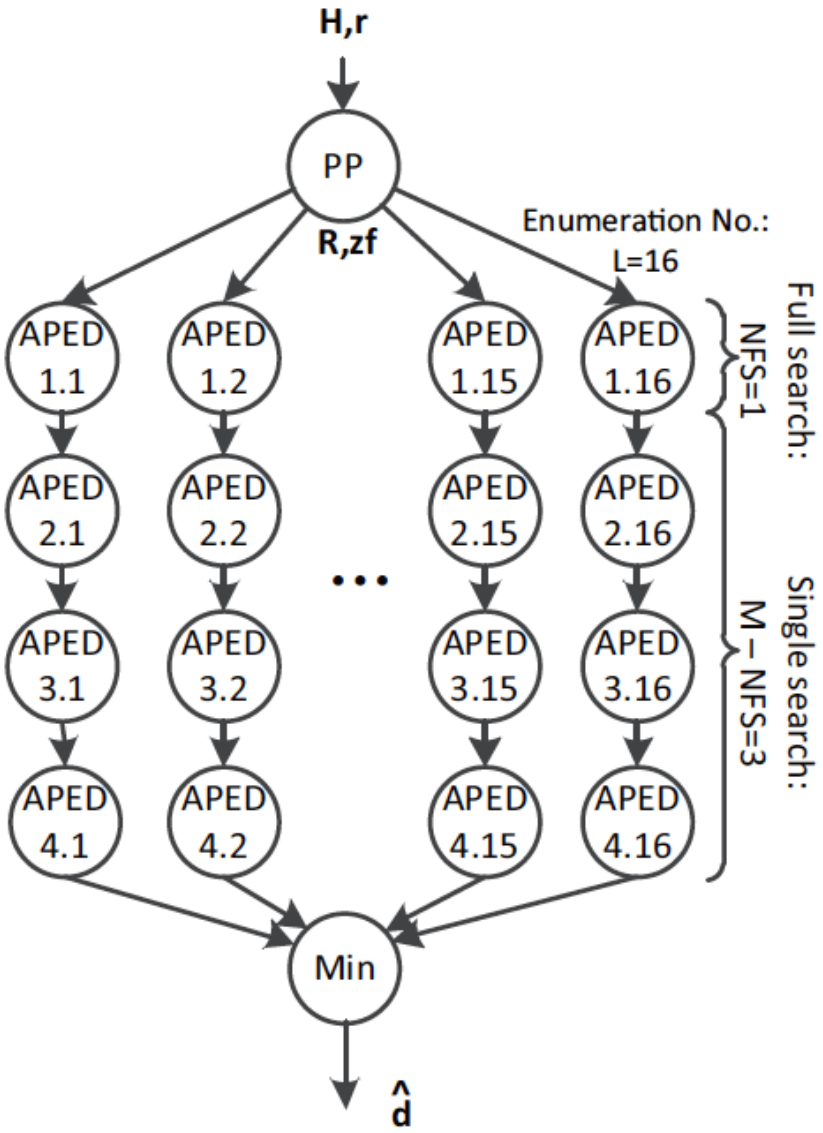


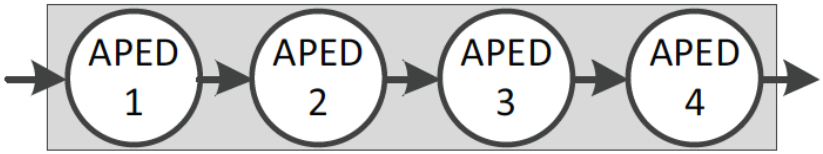

| Config | LUTs | DSP48Es | Latency (cycles) | Clock (MHz) | Throughput (MMACs) |
|---|---|---|---|---|---|
| 16 R | 90 | 1 | 4 | 483 | 483 |
| 16 C | 132 | 1 | 7 | 476 | 119 |
| | 172 | 2 | 5 | 453 | 226.5 |
| | 140 | 4 | 5 | 474 | 474 |
| 32 R | 185 | 2 | 6 | 431 | 215.5 |
| | 182 | 3 | 7 | 431 | 431 |

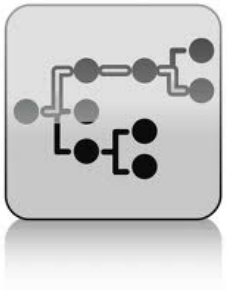

Branch Detection
PC
Zero-overhead Loop
PM
ID
IMM
RF
DSP48E
Coprocessor
ALU
DM
COMM
Branch Control
Instruction Fetch
ID/RF
Source Select
EXE1
EXE2
Result Select
Write Back
FPE
RF
ALU
IMM
PC
PM
ID



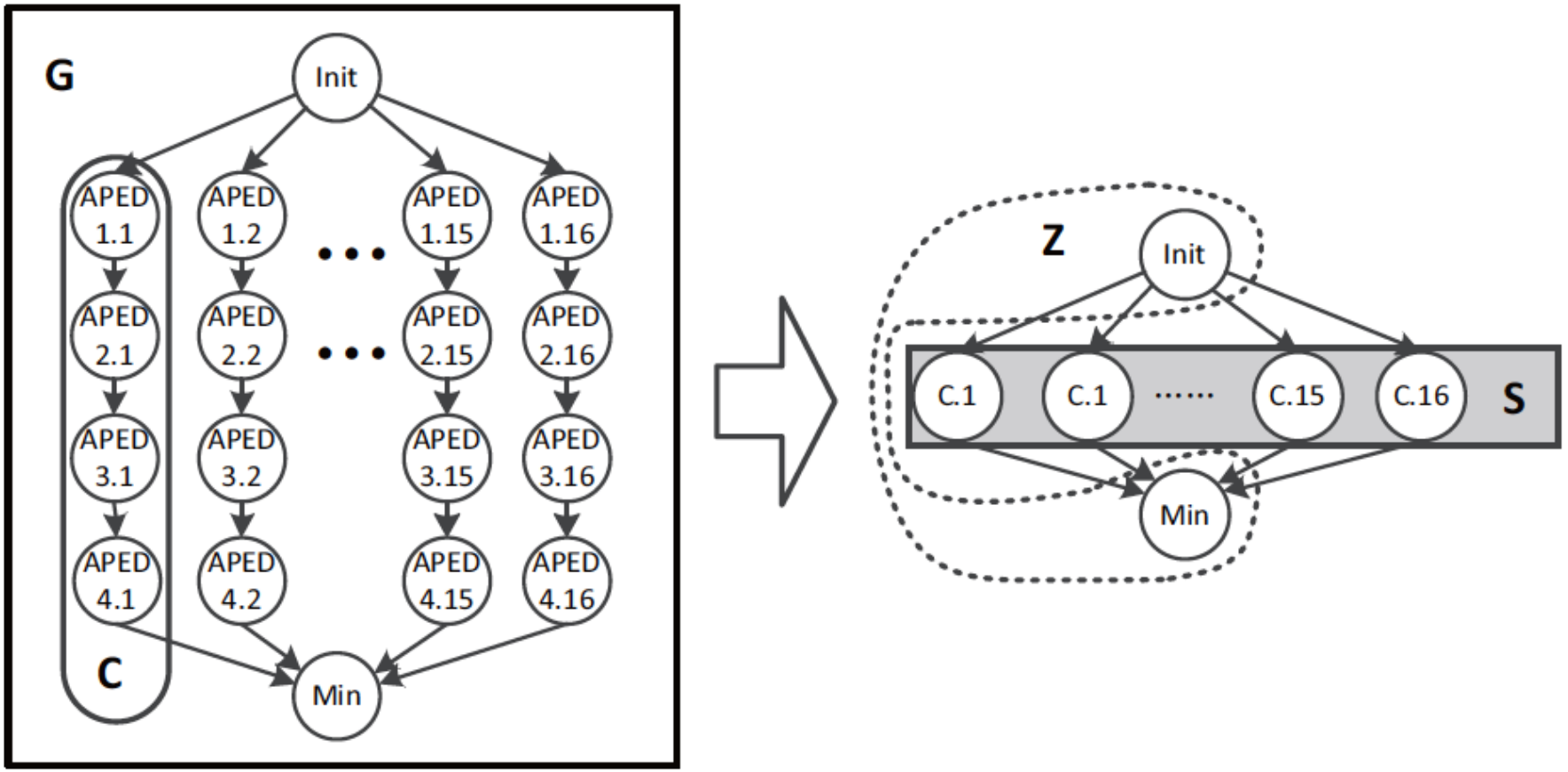

| | |
|---|---|
| LUTs | **96,115** |
| DSP48Es | 408 |
| Clock (MHz) | 189 |
| T (Mbps) | 483 |
| L ($x10^{-6}$ s) | 2.3 |

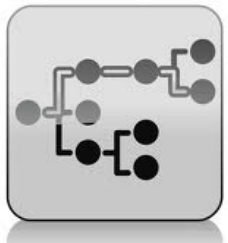

H,r
PP
R,zf
Enumeration No.:
L=16
APED 1.1
APED 1.2
APED 1.15
APED 1.16
APED 2.1
APED 2.2
APED 2.15
APED 2.16
APED 3.1
APED 3.2
APED 3.15
APED 3.16
APED 4.1
APED 4.2
APED 4.15
APED 4.16
Full search:
NFS=1
Single search:
M – NFS=3
Min
d̂

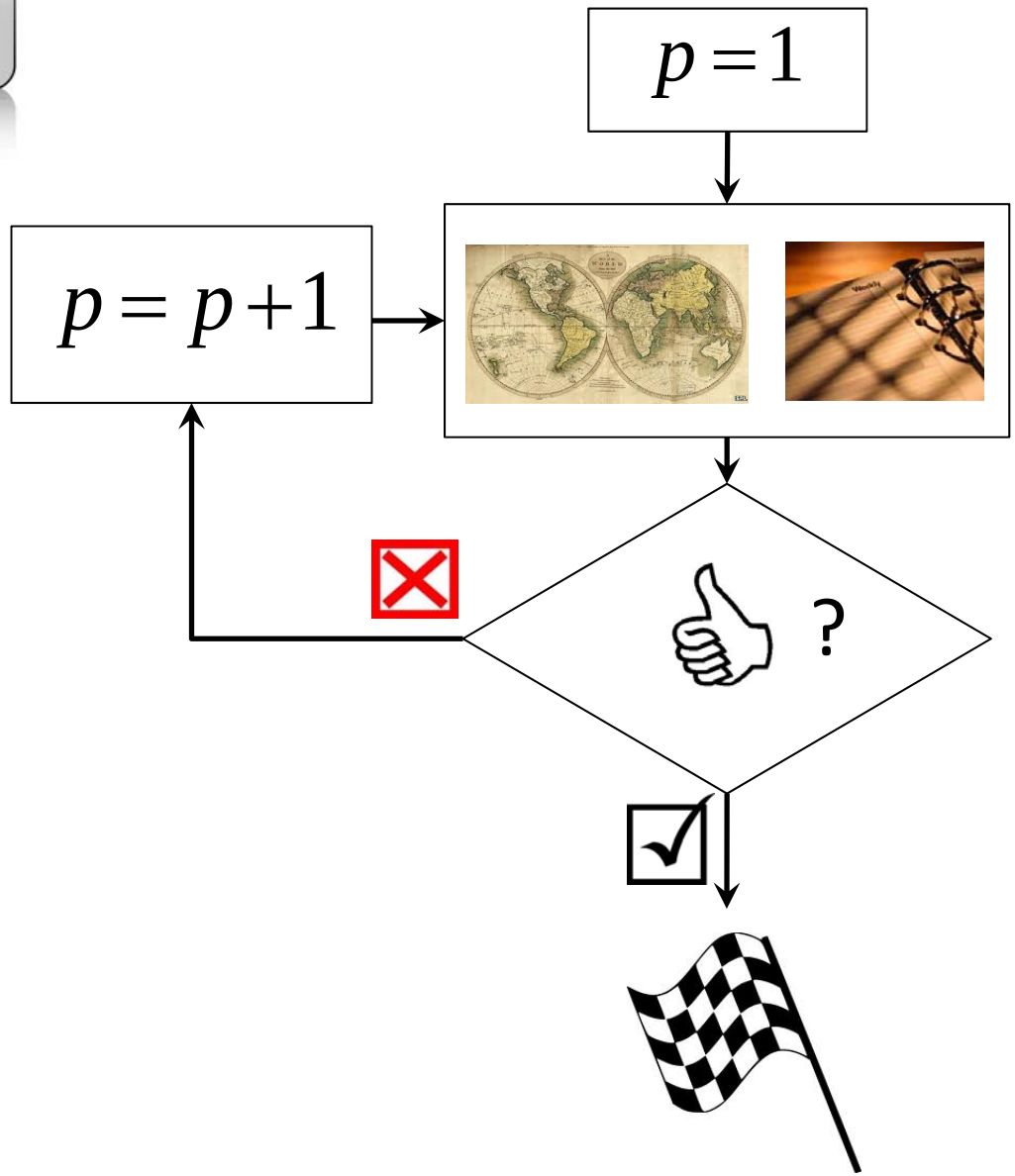

APED 1
APED 2
APED 3
APED 4

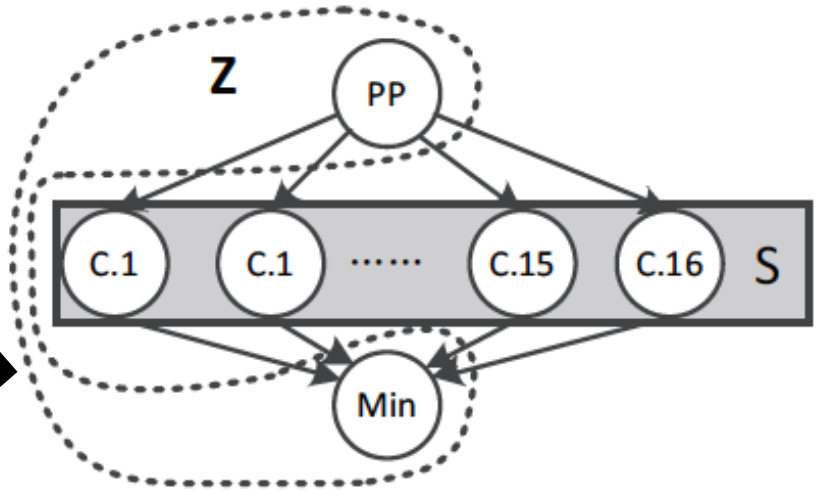


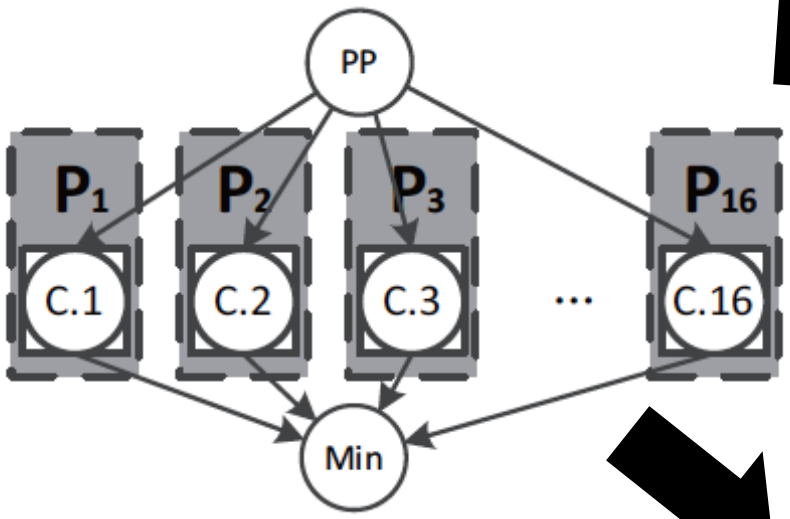

Weekly

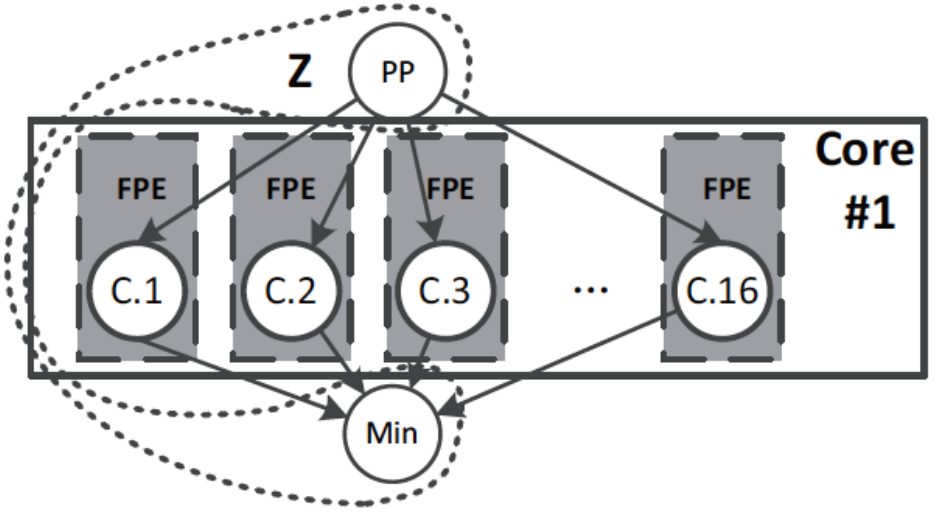

G
Init
APED 1.1
APED 1.2
APED 1.15
APED 1.16
APED 2.1
APED 2.2
APED 2.15
APED 2.16
APED 3.1
APED 3.2
APED 3.15
APED 3.16
APED 4.1
APED 4.2
APED 4.15
APED 4.16
C
Min
Z
Init
C.1
C.1
C.15
C.16
S
Min



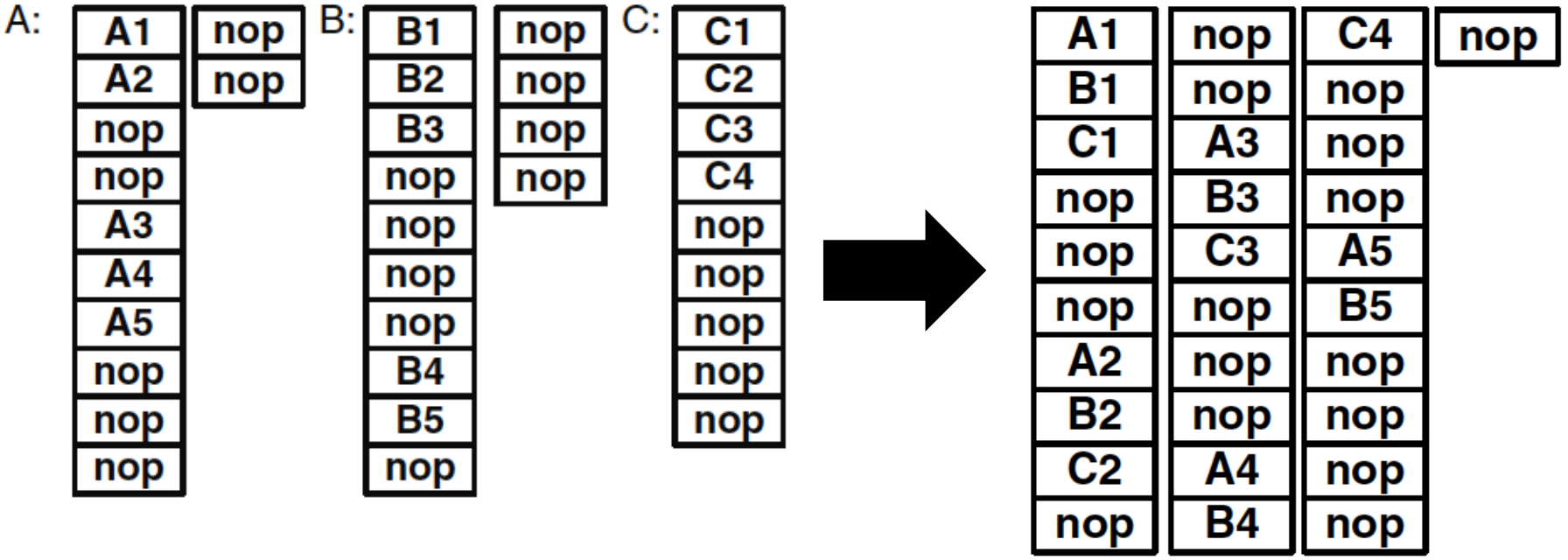

$p = 1$
$p = p + 1$
?

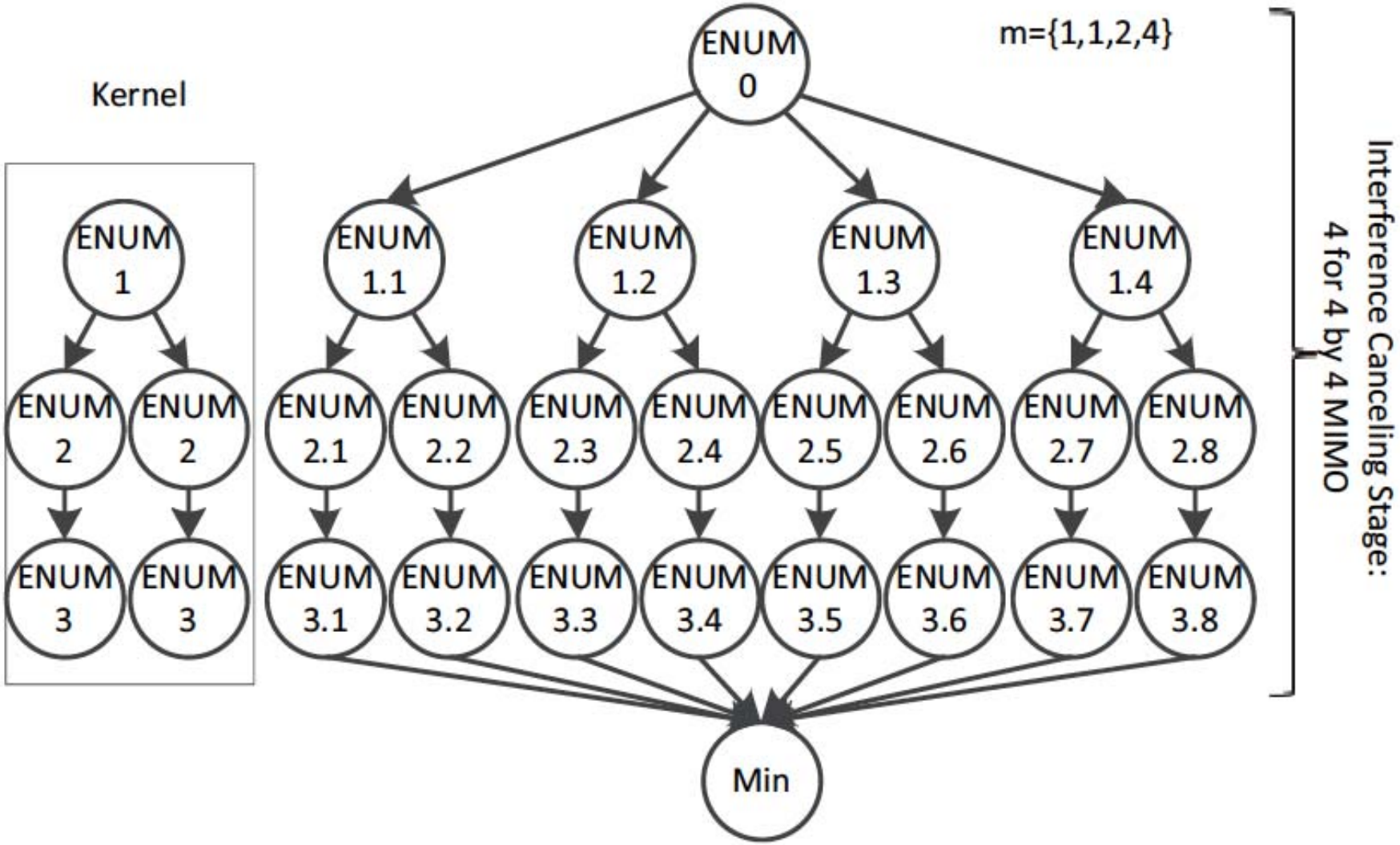

Z
PP
C.1
C.1
.....
C.15
C.16
S
Min


PP
P1
P2
P3
P16
C.1
C.2
C.3
...
C.16
Min


Z
PP
Core
#1
FPE
FPE
FPE
FPE
C.1
C.2
C.3
...
C.16
Min

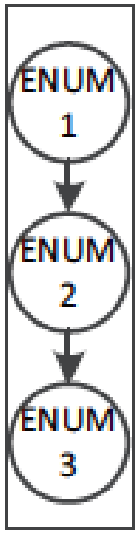

Weekly


A:
A1
A2
nop
nop
A3
A4
A5
nop
nop
nop
nop
nop
B:
B1
B2
B3
nop
nop
nop
B4
B5
nop
nop
nop
nop
C:
C1
C2
C3
C4
nop
nop
nop
nop
A1
B1
C1
nop
B3
C3
nop
nop
A2
B2
C2
nop
nop
nop
A3
nop
nop
A4
B4
C4
nop
nop
A5
B5
nop
nop
nop
nop
nop

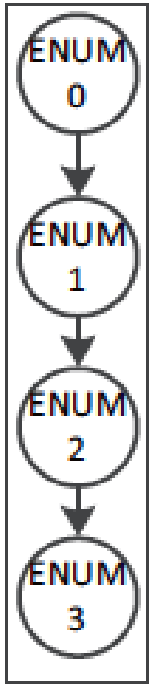

Kernel
ENUM 0
m={1,1,2,4}
ENUM 1
ENUM 1.1
ENUM 1.2
ENUM 1.3
ENUM 1.4
ENUM 2
ENUM 2
ENUM 2.1
ENUM 2.2
ENUM 2.3
ENUM 2.4
ENUM 2.5
ENUM 2.6
ENUM 2.7
ENUM 2.8
ENUM 3
ENUM 3
ENUM 3.1
ENUM 3.2
ENUM 3.3
ENUM 3.4
ENUM 3.5
ENUM 3.6
ENUM 3.7
ENUM 3.8
Min
Interference Canceling Stage:
4 for 4 by 4 MIMO

m={1,1,1,8}

m={1,1,1,4}

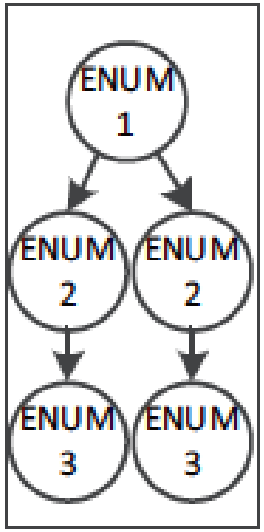



m={1,1,1,1}

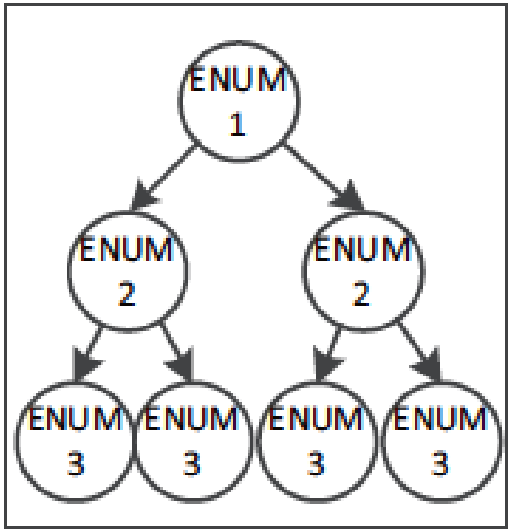



m={1,1,2,8}

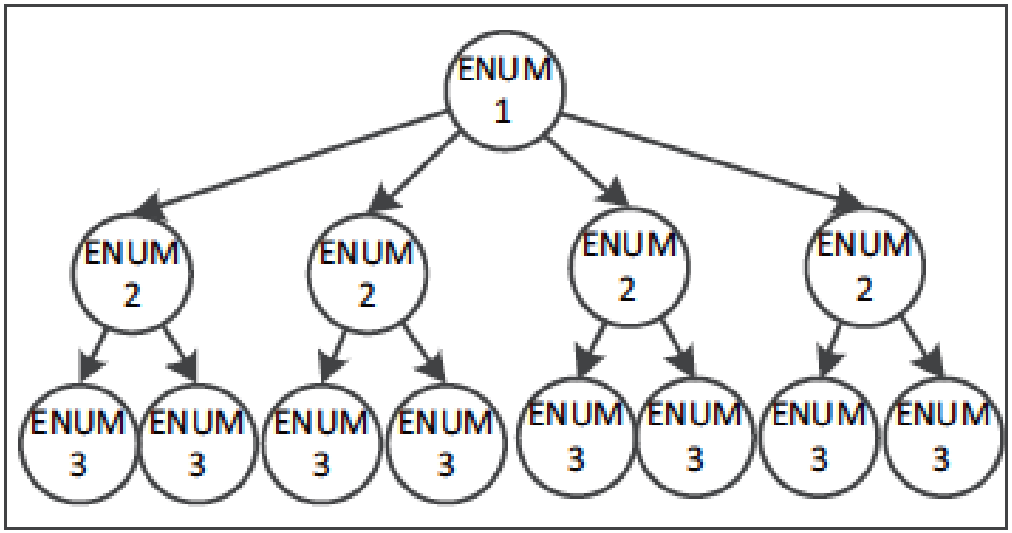
m={1,1,2,4}




m={1,2,2,4}




m={1,2,4,8}



**4 x 4 16 QAM SSFE**

| Scheme | [1,1,1,1] | [1,1,1,4] | [1,1,2,4] | [1,2,2,4] | [1,1,1,8] | [1,1,2,8] | [1,2,4,8] |
|---|---|---|---|---|---|---|---|
| SIMDs | 1 | 3 | 5 | 8 | 5 | 9 | 40 |
| DSP48E1 | 16 | 48 | 64 | 128 | 64 | 144 | 640 |
| LUTS | 2141 | 8531 | 14218 | 22748 | 14218 | 24415 | 113191 |
| Clk (MHz) | 341 | 339 | 318 | 314 | 318 | 322 | 255 |
| Throughput (Mbps) | 618.6 | 482.3 | 498.9 | 521.4 | 510.1 | 489.9 | 500.8 |
| Latency (cycles) | 141 | 225 | 214 | 308 | 314 | 357 | 545 |

**4 x 4 64 QAM SSFE**

| Scheme | [1,1,1,1] | [1,1,1,4] | [1,1,2,4] | [1,2,2,4] | [1,1,1,8] | [1,1,2,8] | [1,2,4,8] |
|---|---|---|---|---|---|---|---|
| SIMDs | 1 | 2 | 3 | 5 | 3 | 6 | 20 |
| DSP48E1 | 16 | 32 | 48 | 80 | 48 | 96 | 320 |
| LUTS | 2141 | 5669 | 8531 | 14218 | 8531 | 17020 | 56593 |
| Clk (MHz) | 341 | 339 | 339 | 333 | 339 | 315 | 276 |
| Throughput (Mbps) | 927.9 | 581.3 | 547.1 | 520.1 | 489.3 | 508.5 | 485.9 |
| Latency (cycles) | 141 | 168 | 357 | 308 | 499 | 357 | 545 |

**4 x 4 FSD**

| Modulation | 16-QAM | 64-QAM |
|---|---|---|
| SIMDs | 9 | 10 |
| DSP48E1 | 144 | 160 |
| LUTS | 24415 | 27802 |
| Clk (MHz) | 322 | 298 |
| Throughput (Mbps) | 503.3 | 500.9 |
| Latency (cycles) | 184 | 184 |